

Claims:

- 1 1. A system to perceive an event-triggering command, the system comprising:  
2 a first device to perceive said command upon detection of a predetermined sequence of  
3 relevant data values within a string of data values, said string of data values including said relevant  
4 data values and a number of non-relevant data values, if said string of data values includes 'N' or  
5 less non-relevant data values between any two sequential relevant data values.
- 1 2. The system of claim 1, further comprising a tap line to communicate said string of data  
2 values between a signal line and said first device.
- 1 3. The system of claim 2, wherein the event comprises switching between a communication  
2 path between the first device and a third device and a communication path between the signal line  
3 and the third device.
- 1 4. The system of claim 3, wherein the first device is a logic device, the third device is a memory  
2 device, and said data values are memory addresses.
- 1 5. The system of claim 4, wherein the logic device is a Field Programmable Gate Array  
2 (FPGA).
- 1 6. The system of claim 4, wherein the memory device is Synchronous Dynamic Random  
2 Access Memory (SDRAM).

1 7. The system of claim 1, wherein said command is perceived by a data value sequence  
2 detector.

1 8. The system of claim 7, wherein said detector includes a plurality of value sequencing units.

1 9. The system of claim 8, wherein each value sequencing unit includes at least one comparator  
2 communicatively coupled to at least one counter.

1 10. The system of claim 9, wherein each value sequencing unit is associated to a different  
2 relevant data value in the sequence of relevant data values.

1 11. The system of claim 10, wherein upon recognition of a first relevant data value in the  
2 sequence, by a first value sequencing unit associated to a first relevant data value, an associated first  
3 counter resets and then progresses one counter state for each of a plurality of clocking signals, until  
4 'N+2' counter states have passed by said first counter.

1 12. The system of claim 11, wherein, upon recognition of a second relevant data value, by an  
2 associated second value sequencing unit, before said first counter passes 'N+2' counter states, said  
3 second counter resets and then progresses one counter state for each of said clocking signals, until  
4 'N+2' counter states have passed by said second counter.

1 13. The system of claim 12, wherein, upon recognition of a third relevant data value, by an  
2 associated third value sequencing unit, before said second counter passes 'N+2' counter states, said

3 third counter resets and then progresses, one counter state for each of said clocking signals until  
4 'N+2' counter states have passed by said second counter.

1 14. The system of claim 12, wherein upon recognition of a last relevant data value in the  
2 sequence after sequential recognition of all other relevant data values, the event-triggering command  
3 is perceived.

1 15. A method to perceive an event-triggering command, the method comprising:  
2 perceiving, by a first device, said command upon detection of a predetermined sequence of  
relevant data values within a string of data values, said string of data values including said relevant  
data values and a number of non-relevant data values, if said string of data values includes 'N' or  
less non-relevant data values between any two sequential relevant data values.

1 16. The method of claim 15, wherein a tap line is to communicate said plurality of data values  
between a signal line and said first device.

1 17. The method of claim 16, wherein the event includes switching between a communication  
2 path between the first device and a third device and a communication path between the signal line  
3 and the third device.

1 18. The method of claim 17, wherein the first device is a logic device, the third device is a  
2 memory device, and said data values are memory addresses.

- 1 19. The method of claim 18, wherein the logic device is a Field Programmable Gate Array  
2 (FPGA) and the memory device is Synchronous Dynamic Random Access Memory (SDRAM).
- 1 20. The method of claim 15, wherein said command is perceived by a data value sequence  
2 detector.
- 1 21. The method of claim 20, wherein said detector includes a plurality of value sequencing units.
- 1 22. The method of claim 21, wherein each value sequencing unit includes at least one  
2 comparator communicatively coupled to at least one counter.
- 1 23. The method of claim 22, wherein each value sequencing unit is associated to a different  
2 relevant data value in the sequence of relevant data values.
- 1 24. The method of claim 23, wherein upon recognition of a first relevant data value in the  
2 sequence, by a first value sequencing unit associated to a first relevant data value, an associated first  
3 counter resets and then progresses, one counter state for each of a plurality of clocking signals, until  
4 'N+2' counter states have passed by said first counter
- 1 25. The method of claim 24, wherein, upon recognition of a second relevant data value, by an  
2 associated second value sequencing unit, before said first counter passes 'N+2' counter state, said  
3 second counter resets and then progresses, one counter state for each of said clocking signals, until  
4 'N+2' counter states have passed by said second counter.

1 26. The method of claim 25, wherein, upon recognition of a third relevant data value, by an  
2 associated third value sequencing unit, before said second counter passes 'N+2' counter states, said  
3 third counter resets and then progresses, one counter state for each of said clocking signals until  
4 'N+2' counter states have passed by said second counter.

1 27. The method of claim 25, wherein upon recognition of a last relevant data value in the  
2 sequence after sequential recognition of all other relevant data values, the event-triggering command  
3 is perceived.

1 28. A system to perceive an event-triggering command, by a logic device, the system  
2 comprising:

3 a signal line to communicate a plurality of memory addresses between a host and one or  
4 more second devices; and

5 a logic device coupled to said signal line to perceive said command upon detection of a  
6 predetermined sequence of relevant memory addresses within a string of memory addresses on said  
7 signal line, said string of memory addresses including said relevant memory addresses and a number  
8 of non-relevant memory addresses, if said string of memory addresses includes 'N' or less non-  
9 relevant memory addresses between any two sequential relevant memory addresses.

1 29. The system of claim 28, wherein the event comprises switching between a communication  
2 path between the logic device and a memory device and a communication path between the signal  
3 line and the memory device.

- 1 30. The system of claim 29, wherein the logic device is a Field Programmable Gate Array  
2 (FPGA) and the memory device is Synchronous Dynamic Random Access Memory (SDRAM).

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